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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,921	12/10/2001	Robert Thomas Bailis	RPS920010132US1	5851

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EXAMINER
DINH, PAUL

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·D

Office Action Summary	Application No.	Applicant(s)	
	10/015,921	BAILIS ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This FINAL OFFICE ACTION is a response to the amendment + remarks filed on 7/5/05.

Claims 1-12 and new claims 13-19 are pending.

Specification

The specification (in Present US patent application publication No. 2003/0110306) is objected to because paragraph 0023 describes reference number 127 as a media access controller (MAC) while figure 1 shows reference number 127 is a PLB arbiter.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

New claims 14, 16 and 18 recite a ROM; therefore, this feature must be clearly shown/labeled in the drawings or this feature canceled from the claims.

NO NEW MATTER SHOULD BE ENTERED

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Leitch (USP 6531889)

(Claim 1 and similarly recited claims 6, 10)

A SOC IC (col 9 line 59, col 4 lines 34-38, 55-58, col 6 lines 17-18, col 7 line 51) comprising:

a plurality of logic functions, the plurality of logic functions including a plurality of base functions (see rejection of claim 11 for base functions) and a plurality of peripheral functions (fig 1-8, 11); and

at least one FPGA cell (embedded trace macro cell 11080 in IC 1005 and FPGA in col 1), coupled to the plurality of peripheral functions, wherein the FPGA cell is configurable

(Cell 11080 is configurable to operate in combination with one or more of: i.e.,
(Col 4-5) re-configurable logic circuitry, embedded controller circuitry, programmable/ reconfigurable storage circuitry, data for configuration, re-programming and re-configuration, routines for initialization and interrupting
(Col 6-7) arbitration mechanism, arbitration software, processors, SDRAM, SDRAM controller,
(Col 10-14) register, power-on-reset circuitry and specification, media-access Control (MAC, Initialization configuration, UART, ROM/PROM/EPROM/EEPROM for configuration,
(Col 20) software for debugging, tracing, and monitoring,
And/or
The hardware, software, instructions in fig 1-8, 11-14)

to selectively enable the plurality of peripheral functions in the field to allow access to the plurality of peripheral functions (fig 1-8) by a customer (*customer = one or more of: "user", "designer" and "system's user" in col 1, 4-6, 9, 13-15, 20*).

(See the following rejection of claims 2 and 7 for the limitations "bus (es), processor local bus (PLB), and on-chip peripheral bus (OPB)". in the similarly recited claims 6 and 10)

(Claim 2) a bus (in fig 5-8) coupled to the at least one FPGA cell.

(Claims 3, 8) wherein the FPGA cell is programmed to selectively complete connections from the bus to the peripheral functions or selectively tie the peripheral function to an inactive state (fig 1-8, 11).

(Claims 4, 9) wherein the FPGA cell programs a register (5065 in fig 5-8) coupled thereto.

(Claim 5) wherein the FPGA cell is configurable by as customer (this limitation is inherent and that is what a cell in Field programmable gate array (FPGA) is for, also see col 4 line 48+, col 14 line 54+ for this teaching of customer configured/ modified/updated/stored FPGA cell).

(Claim 7) a plurality of buses (fig 5-8) wherein the plurality of buses comprises a processor local bus (PLB) and an on-chip peripheral bus (OPB); and

(Claim 11) wherein the plurality of base functions comprise any combination of:

a processor (fig 5-6), a universal interrupt controller (col 2 line 1+), an SDRAM controller (col 6 lines 38-39, col 7 lines 25-26), an on-chip controller OCM (col 4 lines 36-38, col 8 line 25+, col 13 line 60, fig 5-8, an SRAM (fig 5-6, 14), a PLB arbiter (col 8 line 80+, col 13 line 45+), an OPB arbiter (col 8 line 80+, col 13 line 45+), an OPB bridge, and a UART (col 14 line 39).

(Claim 12) wherein the plurality of peripheral functions comprise any combination of:

an external bus controller (EBC), an SDRAM controller (col 6 lines 38-39, col 7 lines 25-26), a proprietary function (debugging/tracing/monitoring in col 20), a peripheral controller (col 6 line 37+, fig 1-8, 11), an IsquareC Interface, a second UART, a DMA controller, a media access layer (MAL) function, and a plurality of media access controllers (col 14 line 31+).

(Claims 13, 15, 17) wherein the FPGA cell coupled to the plurality of peripheral functions is configured after power-on reset (POR 5090 in fig 5-8) in a customer application.

(Claims 14, 16, 18) wherein the SOC integrated circuit is coupled to a companion ROM (col 14 line 65) that stores a programming file that selectively enables the plurality of peripheral functions specific to the customer.

(Claim 19) further comprising an enable status register (5065 in fig 5-8) coupled to at least one of the FPGA cells and allowing the determination of which peripheral functions are enabled after power-on reset (POR 5090 in fig 5-8) and before attempting to execute the peripheral functions.

Applicant's arguments with respect to claim1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner

Paul Dinh